We Claim:

1. A circuit configuration for generating current pulses in the supply current of an integrated circuit, comprising:

connections for receiving supply potentials;

at least one switching unit including two complementary controllable switching elements connected in series between said connections for receiving the supply potentials, said two complementary controllable switching elements including a pull-up switching element having a control terminal and a pull-down switching element having a control terminal, said switching unit having an input terminal that is driven by a first control signal having a rising edge and a falling edge, said input terminal connected to said control terminal of said pull-up switching element and said control terminal of said pull-down switching element;

a delay element configured between said input terminal and a control terminal, selected from the group consisting of said control terminal of said pull-up switching element and said control terminal of said pull-down switching element, so that a current pulse is generated in an event selected from the group consisting of the rising edge of the first control signal and the falling edge of the first control signal.

2. The circuit configuration according to claim 1, comprising:

a further switching unit connected upstream of said switching unit;

said further switching unit including two complementary switching elements having control terminals;

said two complementary switching elements forming a junction point therebetween;

said further switching unit having an input terminal directly connected to said control terminals of said complementary switching elements of said further switching unit;

said further switching unit having an output terminal formed by said junction point between said two complementary switching elements;

said switching unit and said further switching unit forming a switching stage having an input terminal defined by said input terminal of said further switching unit; and

said input terminal of said switching stage being driven with the first control signal.

3. The circuit configuration according to claim 2, wherein said further switching unit forms a CMOS inverter circuit.

4. The circuit configuration according to claim 1, wherein said switching unit includes a CMOS inverter circuit.

5. The circuit configuration according to claim 1, comprising:

a plurality of switching units connected in parallel with regard to the first control signal;

a control circuit; and

a plurality of switching devices being driven by said control circuit;

each one of said plurality of said switching devices being for feeding the first control signal to a respective one of said plurality of said switching units.

6. The circuit configuration according to claim 5, wherein said plurality of said switching units are dimensioned to generate current pulses of different magnitudes.

7. The circuit configuration according to claim 6, wherein said plurality of said switching units are formed such that

current pulses are generated at the rising edge of the first control signal.

8. The circuit configuration according to claim 6, wherein said plurality of said switching units are formed such that current pulses are generated at the falling edge of the first control signal.

9. The circuit configuration according to claim 6, wherein:

said plurality of said switching units includes a first group of switching units and a second group of switching units;

said first group of said switching units are formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching units are formed such that current pulses are generated at the falling edge of the first control signal.

10. The circuit configuration according to claim 5, wherein said plurality of said switching units are formed such that current pulses are generated at the rising edge of the first control signal.

11. The circuit configuration according to claim 5, wherein said plurality of said switching units are formed such that current pulses are generated at the falling edge of the first control signal.

12. The circuit configuration according to claim 5, wherein:

said plurality of said switching units includes a first group of switching units and a second group of switching units;

said first group of said switching units are formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching units are formed such that current pulses are generated at the falling edge of the first control signal.

13. The circuit configuration according to claim 5, wherein said control circuit has a signal generator for generating bit patterns for driving said plurality of said switching devices.

14. The circuit configuration according to claim 13, wherein said signal generator is a random number generator.

15. The circuit configuration according to claim 1, comprising:

a plurality of switching units including a first group of switching units and a second group of switching units;

a first switching device for feeding the first control signal to said first group of said switching units;

a second switching device for feeding a second control signal, which is complementary to the first control signal, to said second group of said switching units; and

a control circuit driving said first switching device and said second switching device;

said first group of said switching units being connected in parallel with regard to the first control signal;

said second group of said switching units being connected in parallel with regard to the second control signal;

said first group of said switching units being formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching units being formed such that current pulses are generated at the rising edge of the second control signal.

16. The circuit configuration according to claim 1, comprising:

a plurality of switching stages connected in parallel with regard to the first control signal;

a control circuit; and

a plurality of switching devices being driven by said control circuit;

each one of said plurality of said switching devices being for feeding the first control signal to a respective one of said plurality of said switching stages.

17. The circuit configuration according to claim 16, wherein said plurality of said switching stages are dimensioned to generate current pulses of different magnitudes.

18. The circuit configuration according to claim 17, wherein said plurality of said switching stages are formed such that

current pulses are generated at the rising edge of the first control signal.

19. The circuit configuration according to claim 17, wherein said plurality of said switching stages are formed such that current pulses are generated at the falling edge of the first control signal.

20. The circuit configuration according to claim 17, wherein:

said plurality of said switching stages includes a first group of switching stages and a second group of switching stages;

said first group of said switching stages are formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching stages are formed such that current pulses are generated at the falling edge of the first control signal.

21. The circuit configuration according to claim 16, wherein said plurality of said switching stages are formed such that current pulses are generated at the rising edge of the first control signal.

22. The circuit configuration according to claim 16, wherein said plurality of said switching stages are formed such that current pulses are generated at the falling edge of the first control signal.

23. The circuit configuration according to claim 16, wherein:

said plurality of said switching stages includes a first group of switching stages and a second group of switching stages;

said first group of said switching stages are formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching stages are formed such that current pulses are generated at the falling edge of the first control signal.

24. The circuit configuration according to claim 16, wherein said control circuit has a signal generator for generating bit patterns for driving said plurality of said switching devices.

25. The circuit configuration according to claim 24, wherein said signal generator is a random number generator.

26. The circuit configuration according to claim 1, comprising:

a plurality of switching stages including a first group of switching stages and a second group of switching stages;

a first switching device for feeding the first control signal to said first group of said switching stages;

a second switching device for feeding a second control signal, which is complementary to the first control signal, to said second group of said switching stages; and

a control circuit driving said first switching device and said second switching device;

said first group of said switching stages being connected in parallel with regard to the first control signal;

said second group of said switching stages being connected in parallel with regard to the second control signal;

said first group of said switching stages being formed such that current pulses are generated at the rising edge of the first control signal; and

said second group of said switching stages being formed such that current pulses are generated at the rising edge of the second control signal.